IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (Currently Amended): A thin film transistor array substrate comprising:

an insulating substrate;

a first metallic pattern formed on said ~~insulting~~ insulating substrate;

an insulating film provided on said first metallic pattern;

a semiconductor pattern provided on said insulating film; and

a second metallic pattern provided on said semiconductor pattern;

wherein said second metallic pattern is surrounded by said semiconductor pattern; and

wherein a part of said semiconductor pattern surrounding a source electrode exists only on said first metallic pattern at a source electrode part in a pixel region.

Claim 2 (Canceled).

Claim 3 (Currently Amended): A thin film transistor array substrate comprising:

an insulating substrate;

a gate line formed on said insulating substrate;

a gate insulating film provided on said gate line;

a semiconductor layer provided on said gate insulating film;

a source line, a source electrode and a drain electrode provided on said semiconductor layer; and

a pixel electrode formed on said drain electrode;

wherein said source line, said source electrode and said drain electrode are surrounded by said semiconductor layer;

wherein said pixel electrode is directly in contact with at least a portion of said drain electrode; and

wherein a part of said semiconductor layer surrounding said source electrode exists only on said gate line at a source electrode part in a pixel region.

Claim 4 (Currently Amended): A thin film transistor array substrate comprising:

an insulating substrate;

a gate line formed on said insulating substrate;

a gate insulating film provided on said gate line;

a semiconductor layer provided on said gate insulating film;

a source line, a source electrode and a drain electrode provided on said semiconductor layer;

an inter-layer insulating film formed on said source line, said source electrode and said drain electrode; and

a pixel electrode formed on said inter-layer insulating film;

wherein said source line, said source electrode and said drain electrode are surrounded by said semiconductor layer;

wherein said inter-layer insulating film is provided with a first contact hole, a second contact hole and a third contact hole, said first contact hole penetrating said inter-layer insulating film to reach said drain electrode, said second contact hole extending to said source line through said inter-layer insulating film, said third contact hole extending to said gate line through said gate insulating film and said inter-layer insulating film; ~~and~~

wherein said first contact hole, said second contact hole and said third contact hole are covered with a pattern made of a material of said pixel electrode; and

wherein a part of said semiconductor layer surrounding said source electrode exists only on said gate line at a source electrode part in a pixel region.

Claims 5-28 (Canceled).